Sheet 1 of 1 PTO
10/033394
12/28/01

U.S. **UTILITY** Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10033394	12/28/2001	438	563	2812	

**APPLICANTS: Lee Seong-jae; Cho Won-ju; Park Kyoung-wan;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
REPUBLIC OF KOREA 01-66742 10/29/2001

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐

Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO.
35 USC 119 conditions met	☐ yes ☐ no	2013p006
Verified and Acknowledged Examiner's initials		

TITLE : Method of fabricating integrated circuit having shallow junction

U.S. DEPT. OF COMM. PAT. & TM. (PO-436) Rev. 10-94

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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